Amendments to the Claims:

This listing of claims will replace all prior versions, and listing, of claims in the application:

Listing of Claims:

1-10. (canceled)

11. (currently amended) A method of manufacturing a semiconductor device, comprising:

~~forming an insulating layer on a substrate;~~

forming a fin structure on ~~the~~ an insulating layer, the fin structure including a first side surface, a second side surface, and a top surface and having a thickness ranging from about 300 Å to about 1500 Å;

forming source and drain regions at ends of the fin structure;

depositing a gate material over the fin structure to a thickness ranging from about 300 Å to about 1500 Å, the gate material surrounding the top surface and the first and second side surfaces;

etching the gate material to form a first gate electrode and a second gate electrode on opposite sides of the fin; and

planarizing the deposited gate material proximate to the fin.

12. (currently amended) The method of claim 11, wherein the forming source and drain regions comprises:

depositing a layer of silicon, germanium, or combination of silicon and germanium, and

patterning and etching the deposited layer to form the source and drain regions, the method further comprising:

implanting impurities in the source and drain regions; and

annealing the semiconductor device to activate the source and drain regions.

13. (currently amended) The method of claim 11, further comprising:

forming a dielectric layer over the top surface of the fin structure, the dielectric layer having a thickness ranging from about 150 Å to about 600 Å.

14. (original) The method of claim 13, wherein the planarizing includes:

polishing the gate material so that no gate material remains above the dielectric layer.

15. (currently amended) The method of claim 11, further comprising:

growing oxide layers on the first side surface and the second side surface of the fin structure, the oxide layers having a thickness ranging from about 10 Å to about 50 Å.

16-20. (canceled)

21. (currently amended) A method of manufacturing a semiconductor device, comprising:

forming a fin on an insulating layer, the fin including side surfaces and a top surface and having a height ranging from about 300 Å to about 1500 Å;

depositing a gate material over the fin, the gate material having a thickness ranging from about 300 Å to about 1500 Å;

etching the gate material to form a first gate electrode and a second gate electrode on opposite sides of the fin; and

removing the deposited gate material from over the top surface of the fin.

22. (previously presented) The method of claim 21, further comprising:

forming source and drain regions at ends of the fin;

implanting impurities in the source and drain regions; and

annealing the semiconductor device to activate the source and drain regions.

23. (currently amended) The method of claim 21, further comprising:

forming a dielectric cap on the top surface of the fin, the dielectric cap having a thickness ranging from about 150 Å to about 600 Å.

24. (previously presented) The method of claim 23, wherein the removing includes:

polishing the gate material down to the dielectric cap.

25. (currently amended) The method of claim 21, further comprising:

growing oxide layers on the opposite sides of the fin, the oxide layers having a thickness ranging from about 10 Å to about 50 Å.

26. (currently amended) A method of manufacturing a semiconductor device, comprising:

forming a fin having a height ranging from about 300 Å to about 1500 Å on an insulating layer;

forming gate dielectric layers having a thickness ranging from about 10 Å to about 50 Å on opposite sides of the fin;

depositing a gate material having a thickness ranging from about 300 Å to about 1500 Å over the fin and proximate the gate dielectric layers;

etching the gate material to form a first gate electrode and a second gate electrode on the opposite sides of the fin; and

removing a portion of the deposited gate material to electrically separate the first gate electrode from the second gate electrode.

27. (currently amended) The method of claim ~~21~~ 26, further comprising:

forming source and drain regions at ends of the fin;

implanting impurities in the source and drain regions; and

annealing the semiconductor device to activate the source and drain regions.

28. (previously presented) The method of claim 26, further comprising:

forming a dielectric cap on a top surface of the fin.

29. (previously presented) The method of claim 28, wherein the removing includes:

polishing the gate material down to the dielectric cap.

30. (canceled)

31. (canceled)